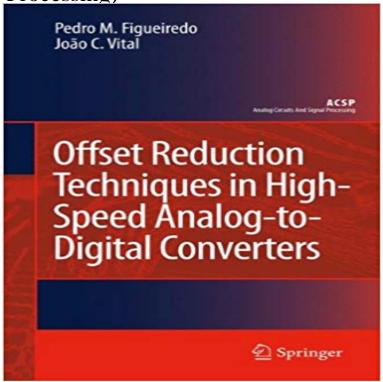
Offset Reduction Techniques in High-Speed Analog-to-Digital Converters: Analysis, Design and Tradeoffs (Analog Circuits and Signal

<u>Processing)</u>



Offset Reduction **Techniques** in High-Speed Analog-to-Digital Convertersanalyzes, describes the design, and presents test results Analog-to-Digital Converters (ADCs) employing the three main high-speed architectures: flash, two-step flash and folding and interpolation. The advantages and limitations of each one are reviewed, and the techniques employed to improve their performance are discussed.

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