

Practical Formal Methods for Hardware Design (Research Reports Esprit)



Formal methods for hardware design still find limited use in industry. Yet current practice has to change to cope with decreasing design times and increasing quality requirements. This research report presents results from the Esprit project FORMAT (formal methods in hardware verification) which involved the collaboration of the enterprises Siemens, Italtel, Telefonica I+D, TGI, and AHL, the research institute OFFIS, and the universities of Madrid and Passau. The work presented involves advanced specification languages for hardware design that are intuitive to the designer, like timing diagrams and state based languages, as well as their relation to VHDL and formal languages like temporal logic and a process-algebraic calculus. The results of experimental tests of the tools are also presented.

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